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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,171	07/23/2003	Thomas Novet	200210020-1	9712
22879	7590	08/09/2005	EXAMINER	
HEWLETT PACKARD COMPANY P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION FORT COLLINS, CO 80527-2400			RICHARDS, N DREW	
			ART UNIT	PAPER NUMBER
			2815	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/626,171

Applicant(s)

NOVET ET AL.

Examiner

N. Drew Richards

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 May 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,4-7,9-12,14-38 and 44-47 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,4-7,10-12,14-38 and 44-47 is/are rejected.
- 7) ☒ Claim(s) 9 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Upon further review, it has been determined that the previously indicated allowable subject matter is not allowable in view of newly found references. These new references are cited herein and fully explained in the rejections below.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 5, 10-12, 14, 15, 18-23, 28, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyamoto et al. ("MIS Emitter with Epitaxial CaF₂ Layer as Insulator", Technical Digest of IVMC '97 Kyongju, Korea 1997, Pp. 226-230) in view of Yoshizawa et al. (U.S. Patent No. 6,472,803 B1).

Miyamoto et al. teach a method for making a flat emitter on page 227 under the heading "Fabrication Process" and as shown in figure 2, for example.

With regard to claim 1, Miyamoto et al. teach:

- defining an emission region in a single crystal electron source (the emission region is defined by the opening in the patterned SiO₂ layer; the electron source is the n+ Si substrate, though not explicitly disclosed it is understood in the semiconductor art that unless otherwise specified a silicon substrate is single crystal);

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- forming at least a first epitaxial layer on the single crystal electron source (the CaF_2 layer is disclosed as being epitaxial as it is formed by molecular beam epitaxy); and
- forming a thin conductor layer on the at least one epitaxial layer (top layer Au is a thin conductor on the epitaxial layer in the emission region).

Miyamoto et al. is silent as to the thin conductor layer (gold layer) being epitaxial. Miyamoto et al. teach depositing the gold layer. Yoshizawa teach an electron emission device that includes an electron source 12, a dielectric layer 13, and an epitaxial gold layer 15 on the dielectric layer in figure 1 for example. Yoshizawa teach the gold layer being epitaxial on column 5 line 61 through column 6 line 5 where they state that MBE (Molecular Beam Epitaxy) can effectively form the layers. It would have been obvious to one of ordinary skill in the art to use the MBE deposition method of Yoshizawa in the device and process of Miyamoto et al. in order to use a known method to form the gold layer where the method is explicitly stated as being an effective method for the deposition.

With regard to claim 5, the at least a first epitaxial layer comprises a dielectric layer (CaF_2 is a dielectric).

With regard to claim 10, Miyamoto et al. teach an electron emitter comprising:

- a single crystal electron source including an emission region (the electron source is the n^+ Si substrate, though not explicitly disclosed it is understood in the semiconductor art that unless otherwise specified a silicon substrate is single

crystal; the emission region is defined by the opening in the patterned SiO₂ layer);

- a thin conductor layer (top layer Au); and
- an epitaxial dielectric layer between the single crystal electron source and the thin conductor layer (the CaF₂ layer is disclosed as being epitaxial as it is formed by molecular beam epitaxy; CaF₂ is a dielectric).

Miyamoto et al. is silent as to the thin conductor layer (gold layer) being epitaxial. Miyamoto et al. teach depositing the gold layer. Yoshizawa teach an electron emission device that includes an electron source 12, a dielectric layer 13, and an epitaxial gold layer 15 on the dielectric layer in figure 1 for example. Yoshizawa teach the gold layer being epitaxial on column 5 line 61 through column 6 line 5 where they state that MBE (Molecular Beam Epitaxy) can effectively form the layers. It would have been obvious to one of ordinary skill in the art to use the MBE deposition method of Yoshizawa in the device and process of Miyamoto et al. in order to use a known method to form the gold layer where the method is explicitly stated as being an effective method for the deposition.

With regard to claim 11, the emitter is operative to emit electrons (disclosed as an electron emitter) substantially free from electric field induced divergence. Though "substantially free from electric field induced divergence" is not explicitly recited by Miyamoto et al., this limitation is considered to be inherently disclosed. The emitted electrons are considered to be "substantially free from electric field induced divergence" as the device of Miyamoto et al. has the same structure as the device thus claimed

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including the epitaxial dielectric layer and single crystal electron source. Since the structures are similar the electrons would be emitted in a similar fashion as in the present invention.

With regard to claim 12, though Miyamoto et al. do not explicitly recite the electrons being emitted from the thin conductor layer at a divergence of less than about 10 degrees from perpendicular, this limitation is considered to be inherently disclosed by the reference. The device of Miyamoto et al. operates in the same fashion as in the instant invention and includes the same structure as in the instant invention. Thus, when the electrons are emitted they will inherently have the same divergence as in the instant application, less than about 10 degrees.

With regard to claim 14, the emitter is operative to generate an electric field across the epitaxial dielectric layer to cause electrons to be emitted from the electron source emission region, to transport through the epitaxial dielectric layer, and to be emitted from the conductor layer substantially free from electrical field induced divergence. The substantially free from electrical field induced divergence is considered taught as discussed above.

With regard to claim 15, since the dielectric layer is formed to a constant thickness (8 nm) and is formed as an epitaxial layer as in the instant invention, it is configured to promote a substantially uniform and unidirectional electric field across its thickness.

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With regard to claim 18, the emission region has a perimeter substantially surrounded by a dielectric (SiO_2 is deposited and etched to form the emission region, thus, the emission region is surrounded by the dielectric SiO_2).

With regard to claims 19 and 20, though Miyamoto et al. do not explicitly disclose the efficiency of their device, since they use the same structure claimed including the flat epitaxial dielectric and the single crystal electron source layer, the device would inherently operate at the claimed at least 6% or 10% efficiency.

With regard to claim 21, the conductor layer (top Au layer) has a substantially flat surface in the emission region that defines an emission surface of the emitter.

With regard to claim 22, the epitaxial dielectric layer is disclosed as having a thickness of less than about 20 nm.

With regard to claim 23, the epitaxial dielectric layer is disclosed as having a thickness of between about 2 and about 10 nm.

With regard to claim 28, Miyamoto et al. teach a thin conductor layer (top Au) but do not teach this layer being less than about 7 nm thick (Miyamoto et al. show the layer being 10 nm thick in figure 2). Nonetheless, it would have been obvious to one of ordinary skill in the art at the time of the invention to form the conductor layer to less than about 7 nm thick. Miyamoto et al. recognize that the gold layer needs to be thin because low scattering in metal is required (a thinner layer will scatter the electrons less). Thus it would have been obvious to form the gold layer even thinner than Miyamoto et al. disclose to further reduce scattering. One of ordinary skill in the art would recognize that the thickness of the gold layer could be reduced until the layer

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became too thin so that it no longer provided the needed conductivity. Providing the layer to about 7 nm or less provides no unexpected result over the prior art and is considered obvious.

With regard to claim 29, Miyamoto et al. disclose under the heading "Measurement" an electrical connection between the single crystal electron source and the thin conductor layer (they attach an Au-wire for front side contact and In-Ga alloy for backside contact and apply a voltage greater than 5V to the emitter), this potential was sufficient to induce an electric field between the conductor layer and the electron source layer to cause electrons to be emitted from the electron source, to transport through the epitaxial layer, and to be emitted from the conductor layer substantially free from electrical field related divergence (since electrons were emitted and measured the potential was great enough to cause the emission; substantially free from electrical field related divergence is considered disclosed by the device as discussed above with regard to claims 12 and 14).

With regard to claim 30, Miyamoto et al. further disclose a target (collector) and the conducting layer configured to direct the emitter electrons towards the target and to cause an effect on the target upon impact (since the electrons reached the target the conducting layer is considered to be configured as claimed and since measurements were taken the emitted electrons inherently had some measurable effect upon the target).

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4. Claims 4, 6, 7, 16, 17 and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyamoto et al. with Yoshizawa as applied to claims 1, 5, 10-12, 14, 15, 18-23, 28, 29 and 30 above, in view of Ossipov et al. (US 2003/0071256 A1).

With regard to claim 4, Miyamoto et al. do not teach forming the single crystal electron source layer on an underlying single crystal electron source layer.

Ossipov et al. teach a flat electron emitter in figure 2B for example, that includes a single crystal electron source layer 230 formed on an underlying single crystal electron source layer 220, a dielectric layer 245, and a thin conductor layer 240 on the dielectric layer. Ossipov et al. refers to this structure as the n⁺-p-D-M structure.

Miyamoto et al. and Ossipov et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the underlying single crystal electron source layer of Ossipov et al. in the method of Miyamoto et al. The motivation for doing so is to provide the n⁺-p-D-M structure to allow high current emission to be combined with stable (durable) operation. Therefore, it would have been obvious to combine Miyamoto et al. with Ossipov et al. to obtain the invention of claim 4.

With regard to claim 6, Miyamoto et al. teach forming an epitaxial dielectric layer but do not teach forming the dielectric layer overlying an epitaxial semi-conductor layer.

Ossipov et al. teach forming the dielectric layer 245 over an epitaxial semi-conductor layer 230.

Miyamoto et al. and Ossipov et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the underlying epitaxial semi-conductor layer of Ossipov et al. in the method of Miyamoto et al. The motivation for doing so is to provide the n⁺-p-D-M structure to allow high current emission to be combined with stable (durable) operation. Therefore, it would have been obvious to combine Miyamoto et al. with Ossipov et al. to obtain the invention of claim 6.

With regard to claim 7, Ossipov et al. teach forming the dielectric layer in the emitter to about 1-5 nm thick and the epitaxial semiconductor layer less than about 20 microns thick.

With regard to claim 16, Miyamoto et al. with Ossipov et al. as combined above teach the single crystal electron source comprising an epitaxial layer 230 formed on a single crystal support 220.

With regard to claim 17, the emission "region" is considered to extend through the thickness of the epitaxial electron source layer to contact the single crystal support. The emission region is considered to be the "region" where the emission occurs, thus an entire cross-section extending down from the top surface is considered the emission "region."

With regard to claim 25, Miyamoto et al. with Ossipov et al. as combined above teach an epitaxial semi-conductor layer 230 sandwiched between the electron source 220 and the epitaxial dielectric layer.

With regard to claim 26, the epitaxial semi-conductor layer is less than about 20 microns thick.

With regard to claim 27, the epitaxial semi-conductor is between about 1 and about 5 microns thick.

5. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miyamoto et al. with Yoshizawa as applied to claims 1, 5, 10-12, 14, 15, 18-23, 28, 29 and 30 above, and further in view of Kaneko et al. (U.S. Patent No. 5,202,605).

Miyamoto et al. does not teach the dielectric being made of one of aluminum nitride or an oxide of silicon, aluminum, tantalum, titanium, hafnium, or zirconium. Yoshizawa teach that the dielectric can be made of these materials in column 5 lines 5-48 but does not provide any motivation for using any of these specific materials. Kaneko et al. teach using a thin insulating layer to allow tunneling of electrons to be emitted. Kaneko et al. teach that the insulating layer should be epitaxially grown of single-crystal material with the crystal planes oriented with respect to the layer surface such as to minimize dispersion of electrons which pass through the insulating layer (column 5 lines 4-11). Kaneko then teach on column 7 line 59 that Al_2O_3 or SiO_2 are suitable as the thin insulating material. It would have been obvious to one of ordinary skill in the art at the time of the invention to use an oxide of aluminum or silicon as the epitaxial dielectric film since they are known to be used as the epitaxial dielectric layer in an electron emitter device because they can be formed to allow the efficiency of electron emission to be increased.

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6. Claims 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyamoto et al. with Yoshizawa as applied to claims 1, 5, 10-12, 14, 15, 18-23, 28, 29 and 30 above, in view of Park et al. (U.S. Patent No. 5736812).

With regard to claim 31, Miyamoto et al. do not teach focusing means positioned between the target and the emitter.

With regard to claim 32, Miyamoto et al. do not further teach the focusing means comprising an electrostatic focusing lens having an aperture in a conductor set at a predetermined voltage, the voltage being adjustable to change the focusing effect of the focusing lens.

Park et al. teach electron guns (electron emitters) that emit the electrons (electron beams) onto a target (phosphor screen). Park et al. teach focusing means (electrostatic focusing lens) positioned between the target and the emitter. The focusing means comprises an electrostatic focusing lens having an aperture in a conductor 12 set at a predetermined voltage, the voltage adjustable to change the focusing effect of the focusing lens. See Park et al. column 1 line 66 through column 2 line 6 and figure 2.

Miyamoto et al. and Park et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to employ a focusing means (specifically the electrostatic focusing lens of Park et al.). The motivation for doing so is so that the emitter of Miyamoto et al. could be used in a display device by focusing the emitted electrons onto

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a phosphor screen. Therefore, it would have been obvious to combine Miyamoto et al. with Ossipov et al. to obtain the invention of claims 31 and 32.

7. Claims 33, 34 and 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyamoto et al. with Yoshizawa as applied to claims 1, 5, 10-12, 14, 15, 18-23, 28, 29 and 30 above, as evidenced by the conventional device of Lee et al. (US 2002/0173153 A1).

With regard to claim 33, Miyamoto et al. teach an electron emitter, and teach that the emitter can be used in microelectronics, but do not teach what applications or devices the emitter can be used in. Electron emitters were known to one of ordinary skill in the art at the time of the invention to be used for memory/storage devices where a memory medium is used as the target.

For example, Lee et al. is evidence that it was conventional to use electron emitter arrays in memory applications. Lee et al. teach the emission target being a memory wherein the effect (caused by the emitted electrons) is a physical change to the target, the physical change being detectable through measurement of electrical properties of the memory. See Lee et al. "BACKGROUND" section. These memory devices of Lee et al. (ASR - Atomic Resolution Storage) are advantageous because they can store a very large number of bits in a small area. Thus, it is well known in the art use electron emitters (such as that taught by Miyamoto et al.) in a storage device.

With regard to claim 34, as evidenced by Lee et al. it was well known to that memory devices using the electron emitters were operable to achieve a density of physical changes of about a terabit per square inch on the memory.

With regard to claim 36, the memory device of Lee et al. includes a mover (mover wafer) connected to one or more of the emitter or the target for moving one or the other of the emitter and the target.

With regard to claim 37, though not explicitly stated, it is nonetheless implicitly understood that the plurality of emitter devices will have control circuitry connected thereto. To allow operation of the emitters and reading and writing of the memory control circuitry must necessarily be connected to the emitter devices.

With regard to claim 38, Lee et al. teach that a plurality of the emitters are arranged in an array including the memory and further including a plurality of focusing lens (focusing electrodes) arranged to cooperate with the array of emitted devices to focus electrons emitted from the devices and to direct the focused electrons towards the memory. Lee et al. further teaches that the focused electrons cause a structural phase change (phase change in the phase change material) in the memory upon impact, these structural phases changes having a density of about a terabit per inch squared in the memory. Lee et al. does not explicitly teach an integrated circuit for detecting the structural phase change through measurement of electrical properties. Nonetheless, it is considered obvious that the phase change will be measured through electrical properties by an integrated circuit. If the phase changes were not measured by an integrated circuit the data stored in the memory array could not be read and would have

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no use. In any memory device, the data that is stored or programmed (in this case the phase change) can be read and processed into a usable output.

8. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miyamoto et al. with Yoshizawa as applied to claims 1, 5, 10-12, 14, 15, 18-23, 28, 29 and 30 above, as evidenced by the conventional device of Cathey, Jr. et al. (U.S. Patent No. 5721560).

Miyamoto et al. teach an electron emitter, and teach that the emitter can be used in microelectronics, but do not teach what applications or devices the emitter can be used in. Electron emitters were known to one of ordinary skill in the art at the time of the invention to be used in display devices where the emitted electrons are absorbed by a phosphor material which then emits visible light. It is known that these display devices have the display as the target for the electron emission and a plurality of pixels where each pixel will undergo a visual change (emit visible light) when the emitted electrons are received by the pixel.

For example, Cathey, Jr. et al. is evidence that it was well known at the time of the invention to use electron emitters display devices. Cather, Jr. et al. provide evidence that it was well known to use a display (screen) with a plurality of pixels as the target where a visual effect is created when the emitted electrons are received by one of the pixels. See for example, column 1 lines 15-36.

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9. Claims 44 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyamoto et al. with Ossipov et al. (US 2003/0071256 A1).

Miyamoto et al. teach in figure 2 an electron emitter device comprising a single crystal electron source (n-Si), a thin conductor (Au), and an epitaxial dielectric (CaF₂) between the single crystal electron source and the thin conductor. Miyamoto et al. do not teach an epitaxial semi-conductor between the electron source and the epitaxial dielectric layer.

Ossipov et al. teach a flat electron emitter in figure 2B for example, that includes an epitaxial semi-conductor 230 formed on an underlying single crystal electron source layer 220, a dielectric layer 245, and a thin conductor layer 240 on the dielectric layer. Ossipov et al. referes to this structure as the n+-p-D-M structure.

Miyamoto et al. and Ossipov et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to an epitaxial semi-conductor between the electron source and the epitaxial dielectric layer of Ossipov et al. in the method of Miyamoto et al. The motivation for doing so is to provide the n+-p-D-M structure to allow high current emission to be combined with stable (durable) operation. Therefore, it would have been obvious to combine Miyamoto et al. with Ossipov et al. to obtain the invention of claim 44. It is noted that layer 230 of Ossipov et al. is not necessarily formed by an "epitaxial" process. However, the use of an epitaxial process is a product-by-process limitation that does not structurally distinguish over the prior art. An epitaxial deposition process is one that results in a layer with the same crystal orientation as that which it is formed

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upon, since layer 230 of Ossipov is a doped region of layer 220, it naturally includes the same crystal structure and thus meets the claim.

With regard to claim 46, the electron source of Miyamoto et al. includes an oxidized region (SiO_2) defining an emission region proximate the oxidized region.

10. Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miyamoto et al. in view of Kaneko et al. (U.S. Patent No. 5,202,605).

Miyamoto teach an electron emitter comprising a single electron source, a thin conductor and an epitaxial dielectric between the single crystal electron source and the thin conductor. However, Miyamoto et al. does not teach the dielectric being made of one of aluminum nitride or an oxide of silicon, aluminum, tantalum, titanium, hafnium, or zirconium. Kaneko et al. teach using a thin insulating layer to allow tunneling of electrons to be emitted. Kaneko et al. teach that the insulating layer should be epitaxially grown of single-crystal material with the crystal planes oriented with respect to the layer surface such as to minimize dispersion of electrons which pass through the insulating layer (column 5 lines 4-11). Kaneko then teach on column 7 line 59 that Al_2O_3 or SiO_2 are suitable as the thin insulating material. It would have been obvious to one of ordinary skill in the art at the time of the invention to use an oxide of aluminum or silicon as the epitaxial dielectric film since they are known to be used as the epitaxial dielectric layer in an electron emitter device because they can be formed to allow the efficiency of electron emission to be increased.

Allowable Subject Matter

11. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

12. Applicant's arguments filed 5/11/05 have been fully considered but they are not persuasive.

Applicant has argued that, with regard to claim 25 and 44, that the Office has incorrectly asserted that region 230 of Ossipov is the epitaxial semiconductor and the single crystal electron source. This is a misinterpretation of the rejection. For claim 25, region 220 is considered the single crystal electron source and region 230 is the epitaxial semiconductor. This interpretation meets the language of the claims. Applicant also argues that region 230 is not taught as being "epitaxial." In response, the examiner points out that claims 25 and 44 are device claims. Epitaxy is a process for forming layers that results in the layer having the same crystal orientation as the layer it is formed upon. However, in a device claim, a specific epitaxial process does not need to be shown, merely the structural result. In this case, Ossipov's layer 230 and 220 necessarily have the same crystal orientation and thus are structurally equivalent to the layers claimed.


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Conclusion

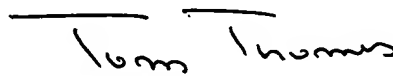
Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



NDR



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SUPERVISORY PATENT EXAMINER